A Comparative Evaluation Of Space Priority Strategies in ATM Networks

and

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Abstract

Current standards reserve one bit in the ATM cell header to indicate loss priority. When congestion occurs at a queue lower priority cells can be discarded in order to insure a smaller cell loss rate for higher priority cells. Strategies for determining which cells to discard are termed space priority buffer management schemes. In this paper two adjustable space priority schemes are studied, where a cell upon arriving to a full buffer can pushout a cell of opposite priority depending upon an adjustable prameter. A queueing analysis of an ATM switching node is conducted to compare the adjustable pushout schemes with other common space priority mechanisms.

1 Introduction

It is well known that for a limited buffer system supporting different classes of traffic, such as an ATM queue at a switch or multiplexor, efficient buffer management schemes are necessary to minimize loss rates. One mechanism for buffer management is the introduction of space priorities among the incoming traffic. Space priority implies that higher priority cells are favored in receiving space in the buffer at a queue. Standards bodies have agreed upon reserving one bit in the ATM cell header to indicate space priority [1]. When congestion occurs at a BISDN queue lower priority cells can be discarded in order to insure a smaller cell loss rate for higher priority cells. Strategies for determining which cells to discard when congestion occurs are termed space priority buffer management schemes or priority cell discarding schemes in the literature. Under the proposed ATM standards, space priority may be implemented in the network at one of two levels, either the connection level or the cell level.

In the case of connection level implementation all cells within a specific connection are given the same space priority which is determined by the type of traffic in the connection. For example, voice can tolerate some loss (e.g. 10^{-6}) with acceptable reproduction still being possible and hence could be marked as low

priority. On the other hand, some types of data traffic may require very low loss rates (e.g. 10^{-8}) and should be given high priority. The space priority would be determined by the connection acceptance algorithm at the time of call set-up, depending on the grade of service required by the connection.

In contrast, for cell level implementation the priority can be different for each cell in an individual connection. The priority can be determined in a number of ways with the priority of the cells being marked either by the traffic source itself or by a bandwidth enforcement device. One approach is to have the traffic source, such as a variable rate subband video encoder, mark the cells on the basis of the information contained in the cell as either essential cells (high priority) or nonessential cells (low priority). An alternate method to cell marking is to have a bandwidth enforcement device such as a virtual leaky bucket determine the priority on the basis of specified traffic parameters. For example, the user negotiates a specified mean rate, peak rate and burst length with the network and as long as the user stavs within the negotiated parameters the virtual leaky bucket tags cells as high priority. However, when the user exceeds the negotiated parameters, the violating cells are marked as low priority and possibly suffer a higher cell loss rate.

Regardless of the implementation of the space priority, the problem at an ATM buffer is the same, namely, how to manage the buffer space to satisfy the loss requirements while maximizing the potential throughput. Here we perform an analysis to compare the two novel *adjustable pushout* schemes we proposed in [10] with the partial buffer sharing scheme and the no-priority case. The performance of these space priority schemes is analyzed for an output buffered nonblocking ATM switch assuming symmetric loading. The performance characteristics of the schemes are studied for a wide range of traffic parameters, and the advantages of the two pushout schemes is demon-

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strated. The results are obtained using an analytical model which is validated via simulation.

2 Space Priority Mechanisms

A considerable amount of work exists on the topic of buffer management for packet switched networks [2-12] and more recently on space priority schemes in particular [2-12]. Recent work has focused on analyzing the management of multiple classes of traffic at a single queue and various space priority mechanisms have been proposed. Some of the schemes proposed include separate buffers for each class [7,8], partial buffer sharing (also called nested threshold) [2-9] and pushout schemes [5-11]. In the separate buffer case each class of traffic is assigned a dedicated buffer and cells are discarded only when the buffer for that class is full. Hence, no special buffer management is required but a queue scheduling or polling mechanism is needed to service the separate buffers. However, incomparison to other schemes, a larger total buffer space is needed to meet a specified set of cell loss requirements since no buffer sharing takes place.

In the partial buffer sharing scheme a common buffer is provided for all classes and the sharing of the buffer is controlled by a set of discarding thresholds. Specifically, let T_i denote the discard threshold for the class i traffic and assume that class i has priority over class i + 1. Buffer access for class i cells is granted if less than T_i buffer spaces are occupied. The class with the highest priority is given access to the entire buffer (i.e. $T_1 = SS$ where SS is the total buffer space). Various cell loss requirements for different loading scenarios can be satisfied by adjustment of the threshold values. Note that this approach is prone to buffer wastage since lower priority cells can be discarded even though the entire buffer space is not occupied. This has motivated the development of pushout schemes where buffer access is always granted as long as the entire buffer space in not full. When the buffer is full, an arriving cell can overwrite any lower priority cell in the buffer; if no lower priority cell is present, then the cell is discarded.

The performance of the three schemes has been analyzed in a series of studies [2-12] for various ATM traffic source models (e.g. Bernoulli, Poisson, etc...) and no single scheme has been proven to be uniformly best. However, we feel that a drawback of the available algorithms is that the proposed pushout schemes do not allow for any adjustment (i.e. tuning) of the cell loss rates among the various classes. Specifically, in the previous studies with two classes of traffic (the primary case of interest) class 1 cells (high priority) always overwrite class 2 cells (low priority). Hence, class 1 traffic may be provided a grade of service exceeding what is required for the given traffic pattern and cell loss requirements. The two novel pushout schemes we proposed in [10] provide for adjustment of cell loss rates among the traffic classes.

The two new schemes are termed the threshold pushout and Pow pushout strategies and are defined in the following for the case of two classes of traffic. For both strategies all cells are admitted until the common buffer space is full. In the threshold pushout scheme the space priority is determined according to a set of overwrite thresholds $[T_1, T_2]$ where we require that the sum of the thresholds equal the total buffer space (i.e $T_1 + T_2 = SS$). A class 1 cell arriving to a full buffer can overwrite a class 2 cell if the number of class 2 cells in the buffer exceeds the threshold T_2 , otherwise the arriving cell is discarded. Similarly, a class 2 cell arriving to a full buffer can pushout a class 1 cell if the number of class 1 cells exceeds the threshold T_1 , otherwise the arriving cell is discarded. Note that $T_1 = SS - T_2$ and by adjustment of T_2 one can vary the cell loss rate provided to the two classes. The Pow pushout scheme is conceptually similar except that the space priority is determined by an overwrite probability P_{ow} . Specifically, a class 1 cell arriving to a full buffer will overwrite a class 2 cell with probability P_{ow} . Conversely, a class 2 cell is granted access to a full buffer via pushing out a class 1 cell with probability $1 - P_{ow}$. Clearly, varying P_{ow} provides a mechanism for adjusting the cell loss rates of the two classes.

3 Performance Evaluation

Consider the $N \times N$ nonblocking output buffered ATM switch illustrated in Figure 1. We analyze the switch under synchronous operation and assume that time is divided into slots of constant length equivalent to one cell transmission time. It is assumed that in any time slot the probability that a cell will arrive at a given input is "p". Successive cell arrivals to an input port and the arrivals at the different ports are assumed to be independent. Hence the arrival process is Bernoulli. We assume that an arbitrary cell at an input port is destined for any of the N output ports with equal probability $\frac{1}{N}$. Thus, $\frac{p}{N}$ is the probability a cell appears at an arbitrary output port in a slot, and the arrival process at output port j $(1 \le j \le N)$ can be characterized as

Prob{k cells arrive at output j during a slot}

$$= \binom{N}{k} \left(\frac{p}{N}\right)^{k} \left(1 - \frac{p}{N}\right)^{N-k} . \tag{1}$$

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The offered load at a link is $\rho = p$. Also, each output port has a finite buffer capable of holding SS cells.

Note that the arrival stream at each input port will have been typed into two space priority classes. Let h= Prob{ an arriving cell is of class '1'} and (1-h) = Prob{ an arriving cell is of class'2'}. Also, let p(l, m)= Prob{ exactly l class '1' cells and m class '2' cells arrive at the output j during a slot }, which is given by

$$p(l,m) = {\binom{N}{l+m}} \left(\frac{p}{N}\right)^{l+m} \left(1-\frac{p}{N}\right)^{N-l-m} \times {\binom{l+m}{l}} (h)^l (1-h)^m .$$
(2)

Defining $\rho_1 = p \times h$ as the offered load for class '1' cells and $\rho_2 = p \times (1-h)$ as the offered load for class '2' cells, we have that the total load $\rho = \rho_1 + \rho_2$.

Consider a single output queue in Figure 1. Let \tilde{X}_1 and \tilde{X}_2 denote the number of class '1'and class '2' cells in the queueing system at the end of a time slot. Let D be the duration of a slot and consider the discrete time discrete state stochastic process defined by $\{(\tilde{X}_1(kD), \tilde{X}_2(kD)) : k = 0, 1, 2, ...\}$, The state space of the process $\{\tilde{X}_1, \tilde{X}_2\}$ is given by the tuple (i, j) $\{(i, j) : 0 \leq i, 0 \leq j, 0 \leq i + j \leq SS\}$. The state probabilities are defined as $\pi_{i,j}^{(k)} = Prob\{(\tilde{X}_1(kD) = i, \tilde{X}_2(kD) = j)\}$. Since the queue is finite, it is stable, and the steady state probability distribution defined as $\pi_{ij} = \lim_{k \to \infty} \pi_{ij}^{(k)}$ exists. Let level n denote the set of steady state probabilities are probabilities.

Let level *n* denote the set of steady state probabilities such that the total number of class '1' and class '2' cells is equal to 'n' that is, $\pi_n = [\pi_{0,n}, \pi_{1,n-1}, \dots, \pi_{n,0}]$ for each $n = 0, 1, \dots SS$. The vector of all state probabilities is then given by: $\pi = [\pi_0, \pi_1, \dots, \pi_{SS-1}, \pi_{SS}]$. The steady state probability vector π can be determined using the well known formula $\pi = \pi \times P$ and the normalization condition $\pi e = 1$, where $e^T = [1, 1, \dots 1]$ and P is the state transition matrix. The state transition matrix will have the following generic form.



Figure 1: N X N Output Buffered Switch

	M _{0,0}	$M_{0,1}$	•••	$M_{0,SS-1}$	$M_{0,SS}$
	$M_{1,0}$	$M_{1,1}$		$M_{0,SS-1}$	M _{1,SS}
	÷	:		:	:
P =	:	:		:	:
	:	:		:	÷
	:	:		÷	:
	M _{SS,0}	$M_{SS,1}$		$M_{SS,SS-1}$	M _{SS,SS}

In the state transition matrix, each $M_{y,x}$ is a submatrix defining the rate of transition from level y to level x and the dimensions of $M_{y,x}$ are $(y+1) \times (x+1)$. Note that, if the number of cells in the system is greater than zero, then a single cell will depart at the end of each slot time and the maximum number of cells that can arrive in any given slot is limited by the switch size (i.e., N). This gives rise to the condition that $M_{y,x}$ is a null matrix if $\{x < (y-1)\}$. Also, the upper bound on the number of cell arrivals in a slot due to the switch size being N causes $M_{y,x}$ to be null for $\{x > (y+N)\}$ as well. Hence we have $M_{y,x} = 0$ if $\{x < (y-1) \text{ or } x > (y+N) \}$. The exact form of the nonnull submatrices $M_{y,x}$ for a specific space priority scheme can be determined by examining the possible state transitions and their associated probabilities.

Consider the no-priority case when there are l class '1' cells and m class '2' cells in the system at the kth instant of time, that is the state of the system is (l, m). Consider a transition to the state (i, j) at the (k + 1)instant such that $0 \le (i + j) < SS$ and $N \ge (i + j) - (l+m) \ge -1$. Thus, there could be transitions only to one level below the current level or a transition to any of the N-1 levels above the current level, depending upon the number of arrivals.

As shown in the Figure 2 the state transition to (i, j) could be achieved by two different cell arrival patterns. The state of the system at the end of the kth instant, when the cell in service during that slot time has been served, will be either (l - 1, m) or (l, m - 1). If a class '1' cell was in service during the kth slot interval, then upon end of service the state of the system would be (l - 1, m). The probability of a class '1' cell being in service would be $P\{$ class '1' cell is in service $\} = \frac{l}{l+m}$. Similarly, if a class '2' cell was in service the state of the system

would be (l, m - 1). The probability of a class '2' cell in service is, $P\{\text{class '2' cell is in service}\} = \frac{m}{l+m}$. Hence, following the first scenario the number of class '1' cells that are required to reach the state (i, j) would then be i - (l - 1). Similarly the the number of class '2' cells required would be j - m. The probability of this arrival pattern can then be found using equation (2) as $P_A = p\{i - l + 1, j - m\}$. Following the second scenario where a type '2' cell is in service it is easy to see that the number of class '1' and class '2' cells required are i - l and j - (m - 1) respectively. The probability associated with this arrival pattern is $P_B = p\{i - l, j - m + 1\}$ and is given by (2).

Now consider the case where the transition is to a state (i, j) at the highest level SS (i.e., the the buffer becomes full: i + j = SS). The determination of the number of cells required for a transition is the same as in the case presented above, except that in the computation of P_A and P_B one must account for the fact that the desired state is reached even if the number of cell arrivals exceeds the exact requirement. This is because all the arrivals after the buffer fills are discarded. Hence P_A and P_B are a weighted sum of multiple arrival probabilities. A weight is associated with the arrival probabilities to ensure that when the total number of arrivals during a slot exceeds the available space in the buffer, both class '1' and class '2' cells are given equal access to the buffer space. Hence,

$$P_{A} = \begin{cases} 0 & \text{i-l+1} \ge 0 \\ j - m \ge 0; \\ i + j - (l + m - 1) \le N \end{cases}$$

$$P_{A} = \begin{cases} 0 & \text{i-l+1} \ge 0 \\ \sum_{y=j-m} \sum_{x=i-l+1}^{N-y} \\ p(x,y) \times \frac{(\frac{i-l+1}{x+y})(\frac{y}{x-y})}{(\frac{i-l+1+j-m}{x+y})} & \text{otherwise} \end{cases}$$

$$P_{B} = \begin{cases} 0 & \text{i-l} \ge 0 \\ j - m + 1 \ge 0; \\ i + j - (l + m - 1) \le N \end{cases}$$

$$P_{B} = \begin{cases} 0 & \text{i-l} \ge 0 \\ j - m + 1 \ge 0; \\ i + j - (l + m - 1) \le N \end{cases}$$

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An analytical expression for the state probabilities π is difficult to obtain. However, one can easily solve for the state probabilities using standard numerical matrix solution techniques. In order to model the other space priority schemes, appropriate modifica-

tions to the state transition matrix are made. For example, only the last column of the state transition matrix P, that is $\begin{bmatrix} M_{0,SS} & M_{1,SS} & \dots & M_{SS,SS} \end{bmatrix}^T$ needs modification when analyzing *pushout* algorithms. This is because the pushout mechanism is invoked only when an arriving cell finds the buffer full. On the other hand, for the case of the partial buffer sharing scheme all submatrices with final transition indices greater than the threshold for lower priority cells will be affected. Specifically, if the threshold is set at $[T_1, T_2]$, all matrices $M_{y,x}$, $\{M_{y,x} : y \ge T_2$ and $x \ge y$, will be affected. Details of the state transition submatrices for the pushout and partial buffer sharing schemes are given in [13].

In order to validate the analytical queueing model, a corresponding simulation model was developed and the results compared. The simulation model was developed in SLAM and the standard method of replications with deletion of the initial transient was used to statistically analyze the output data. The simulation was run until 90% confidence intervals with 1% relative precision were obtained on all performance measures. An extensive set of experiments comparing the throughput, delay, cell loss rates, and queue lengths of the two models is given in [10,13] with representative results reported here.

The system of Figure 1 was studied for various sets of parameters (N, SS, etc..) and the simulation results compared with the corresponding analytical models. Illustrative results are shown in Figures 3-6 for an experiment where N = 2, SS = 7 and the traffic mix was 50% class one and 50% class two (i.e., h=.5). In the experiment the total load was varied over the range $0 \le p \le 1$ in order to construct performance curves. Typical results for the average number in the system and average number of class 1 and class 2 cells in the system versus p are shown in Figures 3-6. In the figures the simulation values are denoted by symbols (e.g., *) whereas the continuous curves represent the analytical results. Note the good agreement between the analytical and simulation results.

Figure 3 shows the behavior of the average number in the system for the no priority case. Since the traffic mixture is (50%, 50%) the average number of class 1 and class 2 cells are equivalent and are half the total number in the system. Figure 4 illustrates typlical behavior of the partial buffer sharing scheme for thresholds $[T_1 = 7, T_2 = 3]$. Observe the total average number in the system is less than in the no priority case, indicating a lower utilization of the buffer. In general, as the threshold for class 2 is increased allowing more buffer space to be shared, the number of class 2 and class 1 cells queued increases. The partial buffer sharing scheme with thresholds $[T_1 = SS, T_2 = SS]$ will correspond to the no priority case.

In Figures 5 the performance of the threshold pushout mechanism with $[T_1 = 6, T_2 = 1]$ is shown. Also, in Figure 6 the behavior of the P_{ow} pushout scheme with $P_{ow} = .7$ is illustrated. Additional results are given in [13], where the effects of varying the threshold and overwrite probabilities in the pushout policies were investigated. It was shown that for the pushout schemes the total number in the system is independent of the threshold/overwrite probability value, but that the percentage mixture of class 1 and class 2 cells is determined by the threshold/overwrite probability setting.

Having validated the analytical models a study was conducted to determine which scheme provided the best performance. Let Δ_i denote the maximum acceptable cell loss rate for class i traffic. Given a set of cell loss requirements (Δ_1, Δ_2) and the traffic mixture (i.e. (% class 1, % class 2)), the total load was varied until the maximum offered load (MOL) that could be supported while still satisfying the loss requirements was determined. Tables 1-3 show typical results of this study for a given set of cell loss requirements with various values of N and SS. Note that several traffic mixtures were considered for each set of loss requirements. In the results listed for the partial buffer sharing and pushout schemes only the best case is given (i.e. the threshold values and overwrite probabilities were varied until the largest MOL was found). From the tables one can clearly see that the two pushout schemes proposed here provide a significant improvement in potential throughput over the partial buffer sharing scheme. The exact amount of throughput improvement depends on N, SS and the traffic mix. Note that the results of Table 1-3 contradicts the prevailing literature where only a slight improvement is to be expected from a pushout scheme [12-14]. This is primarily due to the fact that the optimum pushout scheme for the cases studied was rarely the case of having class 1 traffic always overwrite class 2 traffic.

A board level hardware implementation of the *threshold pushout* scheme for a 8×8 shared medium ATM switch with a buffer of size 256 cells has been developed and is described in [14]. The implementation is done entirely in hardware and the FIFO ordering of packets at the output of the buffer is preserved by using linked lists as pointers for reading out packets. The hardware design was shown to easily run at speeds up to 82.6 Mbps using off the shelf components with

a 12.5 MHz clock. The hardware design is amenable to ASIC implementation. Also, when compared to a board level hardware implementation of the partial buffering scheme the *threshold pushout* implementation provided an improvement in throughput comparable to the values reported in Tables 1-3 ($\approx 15\%$)

However, the hardware for the threshold pushout scheme is more complex than that required for partial buffer sharing, and was estimated to cost roughly four times as much. Thus, it may be preferrable from a cost/implementation standpoint to adopt the partial buffer sharing scheme. For example, consider the case of N = 8, SS = 21 and traffic mix of (60%, 40%) shown in Table 3, where the threshold pushout scheme supports ($\Delta_1 = 10^{-8}, \Delta_2 = 10^{-6}$) upto a MOL of .804. The partial buffer scheme can also be made to support ($\Delta_1 = 10^{-8}, \Delta_2 = 10^{-6}$) at a MOL up to .804 by increasing the buffer size SS to 26 (a 24% increase) and using thresholds $[T_1 = 26, T_2 = 22]$. Note that from a cost/implementation viewpoint, increasing the buffer size may be perferrable. However, increasing the buffer size will result in an increase in the maximum possible delay and delay jitter. Thus it can be argued that using a smaller buffer and the adjustable threshold pushout scheme is advantageous despite additional cost. This is especially true if the buffers are sized based on delay requirements.

4 Conclusions

In this paper, we have analyzed two adjustable pushout space priority schemes for ATM networks namely: threshold pushout and P_{ow} pushout. The distinct advantage of the new schemes is their ability to adjust the cell loss rates between the traffic classes. The superior performance of the pushout schemes when compared with partial buffer sharing was demonstrated. In particular, it was shown that for a given buffer size and traffic mixture, the pushout schemes could support a significantly higher maximum load subject to a specified set of cell loss requirements.

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Figure 2: Determining State Transitions





4c.3.6



Figure 4: Average Number Curves: Nested Threshold Scheme (h=0.5)

Avg. Number





(N)-4				MOL to	r (%cias	# 1,%cl	ass 2) ti	affic m	X.		
(SS)=7.											
	0,100	10,90	20,80	30,70	40,60	50,50	60,40	70,30	80,20	90,10	100,0
No priority	.4376	.3636	.3436	.3324	.3244	.3184	.3136	.3096	.3064	.3032	.3004
Partial Buffer	.4376	.3680	.3520	.3392	.3300	.3232	.3172	.3220	.3144	.3072	.3004
Pushout threshold	.4376	.4412	.4458	.4500	.4556	.4544	.4096	.3744	.3452	.3212	.3004
% improve- ment over Partial Butter	0	19.90	26.59	32.67	38.06	40.59	29.13	16.27	9.80	4.56	0
Pushout with Pow	.4376	.4412	.4452	.4500	.4556	.4536	.4088	.3736	.3448	.3208	.3004
% improve- ment over Partial Butter	0	19.90	26.55	32.67	38.06	40.50	29.05	16.20	9.75	4.50	0

Table 1: MOL for $\triangle_1 = 10^{-8}$, $\triangle_1 = 10^{-6}$

					(Xclas	1,%.01	aa 2) (r	Mc m			
(N)=4.											•
13-(00)	0,100	10,90	20,80	30,70	40,60	50,50	6 , 40	70,30	80, 20	90,10	100,0
No priority	.7992	.7604	.7488	.7420	91 CL.	9462.	9061.	7284	1264	.7244	7226
Pertial Butter	.7992	.7752	Ē	9CLL:	.7882	.7724	21.07	.7876	7804	.7448	122.
Pushout threshold	.7982	.8012	.8032	8056	1904	8 110.	516 .	0909	.74	.7484	822.
% Improve- ment over Pærliel Butter	0	3.35	3.36	4.14	6.10	5.06	6.25	526	1.14	0.23	•
Puehout with Pow	.7982	.8012	5002	8 908.	1906	9116.	8918.	304	Ĩ.	.7460	122
% improve- ment over Partial Butter	•	3.36	3.35	4.14	£.10	5.08	1.25	5.22	1.78	0.20	•

Table 2: MOL for $\triangle_1 = 10^{-8}$, $\triangle_1 = 10^{-6}$

(N) ≖ 8.				NICT PR	(Nelas	a 1,Xel	us 2) (r	affic mi	al l		
{SS)=21	0,100	10,90	20,80	30,70	40,60	50,50	07 [.] 09	70,30	90,2 0	90,1 0	100,0
No priority	7967	7424	M27.	121	1914.	8217.	7096	7064	7040	.7024	8002.
Perdel Buffer	74467	.7424	7296	127.	3914	8217.	3607 .	2707.	7041	.7024	9002.
Pushout Intrachold	7864	7880	.7804	.7928	7860	0008.	9040	N20	.7560	1927.	7008
% Improve- sent vver Partial Sutter	۰	8.14		£7.4	11.06	12.23	13.30	98"11	121	3.42	•
Jushout with	7864	7880	1067.	.7926	998.	9008	9940	0281.	7840	1961.	7008
6 Improve- ment ver Pætial lufter	•	6.14	8.4	9.75	11.05	12.23	13.30	11.99	72.7	3.42	•

Table 3: MOL for $\Delta_1 = 10^{-6}$, $\Delta_1 = 10^{-6}$

4c.3.8